REMARKS

I. Introduction

Applicants again would like to thank Examiner Natnael for the indication of allowance of claims 2, 3, 5, 8 and 11. In response to the Office Action mailed January 25, 2005, Applicants have amended claim 6 so as to further clarify the claimed subject matter. Support for this amendment can be found, for example, in Fig. 9 and at page 13, line 14 to page 14, line 1 of the specification. No new matter has been added.

Furthermore, it is noted that USP No. 6,192,091 to Yamada cited by the Examiner has not yet been indicated on the PTO-892 form that was sent to the Applicants. Accordingly, it is respectfully requested that the foregoing document be expressly made of record and a new PTO-892 form be reissued indicating that the Yamada reference has been made of record therein.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 6 Under 35 U.S.C. § 103

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 6,192,091 to Yamada. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 6 recites in-part outputting the subtraction input value ... for the data ***coinciding with the code pattern*** of segment synchronous signal, and ... outputting said subtraction input value ... as a clock phase error signal only for the data ***positioned*** at the segment synchronous signal.

In the pending rejection, the Examiner reads the subtraction circuit 104 of Yamada as the claimed circuit for subtracting the N^{th} input from the $N+1^{th}$ input, the sign inversion circuit 107 as the claimed circuit for outputting the subtraction value, and the gate 108 as the claimed circuit for outputting a clock phase error signal. However, Applicants respectfully submit that the phase error signal of Yamada is not equivalent to the claimed clock phase error signal, because the phase error signal "f" of Yamada is generated by the sign inversion circuit 107 based on the ***phase error signal*** "e" and the ***alleged subtraction input value*** (a-b). In contrast, in the latch circuit 207 of the present invention, the data is latched by the signal *Sdet*, such that the signal *Sdet* is adjusted in time so as to latch the subtraction input value after the subtraction of the second and third segment synchronous signals of the reception data by the latch circuit 205 (see, e.g., page 13, lines 21-26 of the specification). In other words, the latch circuit 207 of the present invention functions to generate a latched value in accordance with the ***subtraction input value*** output by the subtraction circuit 202 and the ***latched value*** output by the latch circuit 205.

Additionally, the pending rejection merely ***assumes*** that Yamada discloses "outputting the subtraction input value obtained only for the data coinciding with the code pattern of the segment synchronous signal" without providing or identifying any support for the allegation. Moreover, the pending rejection uses that unfounded allegation to further support the allegation that Yamada discloses outputting a clock phase error signal only for the data positioned at the alleged segment synchronous signal. However, it is difficult for the Applicants to provide a proper rebuttal when the pending rejection has not presented any support or rationale presented in support of this allegation. As best understood, the Office Action is apparently assuming that because Yamada allegedly teaches outputting a clock phase error signal via the sign inversion circuit 107, then the alleged subtraction input value used in determining the clock phase error

signal must also be the data coinciding with the code pattern of the alleged segment synchronous signal, or that the alleged clock phase error signal must also be the data positioned at the alleged segment synchronous signal. However, this incomplete analysis ignores the fact that Yamada is silent with regard to providing ***any*** code pattern or data position, let alone disclose outputting ***only*** the data matching the code pattern or data position of the alleged segment synchronous signal.

Furthermore, the Examiner alleges that it would have been a matter of design choice to utilize any symbol as the claimed clock phase error. As a preliminary matter, it is respectfully submitted that an allegation of design choice assumes the underlying feature is disclosed by the prior art except for minor deviations (e.g., changes in shape, size, etc., (*see* **M.P.E.P. § 2144.04(IV)**). Only when the underlying feature is disclosed by the prior art would an allegation of design choice of the minor deviation potentially be proper for an initial grounds of rejection, which can then be rebutted by evidencing a purpose for the deviation.

In the instant case, the Examiner admits that Yamada does not disclose the underlying features themselves (e.g., the second or third symbol), but simply discounts the ***entire*** feature as being obvious design choice. Accordingly, it is respectfully submitted that the Examiner has not established any basis for a proper showing of *prima facie* obviousness, and the assertions of obvious design choice are based solely on improper hindsight reasoning.

Furthermore, as readily discussed at page 8, line 19 to page 9, line 6 and at page 14, line 13 to page 15, line 19 of the specification, the subtraction processing of the present invention is to determine the inclination of the linking line of the sample point values b and c (see, Fig. 6, which are shown to be at the same level). If the frequency or phase of the sample points b and c deviates, the clock phase error signal "Pherr" thereof is determined by the subtraction process.

Specifically, the differential value of all data matching the synchronous signal and the code pattern of the packet data is fed back continuously to the VCO 18 as clock phase error until the segment synchronous signal of the packet is detected. For example, if the signal "Segst" showing the ***position*** of the segment synchronous signal of the data and the signal "Sdet" showing the ***code pattern*** of the segment synchronous signal are the same data, the N^{th} and $N+1^{th}$ synchronous signals of the packet data are processed by subtraction, and the clock phase error signal "Pherr" is determined so that the clock phase error signal can be effectively controlled (e.g., until the error signal becomes zero). That is, according to one exemplary embodiment of the present invention, the clock phrase error signal is output when 1) the pattern of the segment synchronous signal comprising the four symbols (i.e., the four sample points) coincides with that shown in Fig. 7, and 2) the pattern of the segment synchronous signal is positioned at the predetermined position (e.g., at the beginning of the 832 symbols as shown in Fig. 6). Accordingly, the segment synchronous signal contained in the packet can be advantageously detected stably and established precisely and securely even under a poor radiowave condition, such as ghost, multipath or channel interference, for receiving broadcast signals.

In contrast, as discussed *supra*, Yamada is completely silent as to the problems related to the inferior environments under which the signals are detected, let alone the means by which to solve such problems as conceived by Applicants. In this regard, Yamada, at best, is merely cumulative to the admitted prior art described at pages 1-4 of Applicants' specification, because Yamada is also subject to the same drawback with regard to the difficulty of carrying out synchronous signal detection processing, AGC processing and the clock regeneration processing under severe radio wave condition. In this regard, as discussed *supra*, it is respectfully submitted that outputting only the phase errors comprising a second symbol and a third symbol or a first

symbol and a fourth symbol of the segment synchronous signal as the clock phase error is replete with potential purposes, advantages, and/or benefits, and not merely a design choice as alleged in the pending Office Action.

Based on all the foregoing, it is respectfully submitted that claim 6 is patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. § 103 be withdrawn.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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